

Optimization Services For Accelerated Functional Verification Closure

WhizChip offers advanced verification services that enable your design teams to achieve verification closure in a predictable and traceable manner. Delivered as ‘Verification Optimization Services’, this offering maximises the return on your simulation license and CPU investment and shrinks the overall time required to close verification.

Based on the indigenously developed XPlan platform, this service offering has the in-built flexibility to be deployed into any existing design & verification flow at any stage. Our verification Optimization Services are effective not only for verification environment based on languages like SystemVerilog, Vera etc that natively support constraint random verification, but also with Verilog, VHDL and SystemC. This is unique to WhizChip’s offering. XPlan – the underlying technology, operates based on a machine readable verification plan and is non-invasive on the test bench, making it easy to integrate into your existing flow with no overheads.

I
N
T
R
O
D
U
C
T
I
O
N

How does Verification Optimization Services work?

WhizChip provides a web based platform for formal capture, review and refinement of the verification plan. This allows seamless collaboration across geography, and across all stakeholders. We work with the customers’ team through this planning process, and leverage our verification experience and methodology knowledge to bring in rigor and ensure that the plan is comprehensive by construct. Using XPlan, we then process this executable verification plan automatically to generate code in native test bench language for randomization, to generate optimal constraints, and to define coverage points. Our team owns the responsibility to generate the functional stimulus set, run simulations, analyze coverage reports and make refinements to the inputs to achieve the desired goals. The reports and associated verification stimuli are shared with customer teams for review and sign-off.

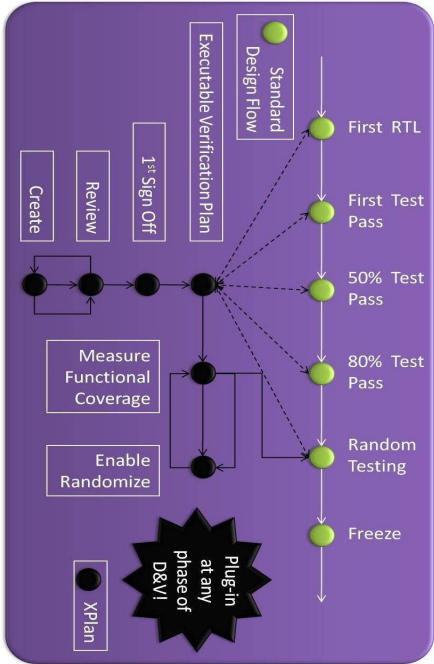
B
E
N
E
F
I
T
S

Key Benefits

- ✓ Save cost and time and close the verification cycle comprehensively by
 - enabling verification planning across multiple sites and across all stakeholders
 - setting platform to capture an executable verification plan and improve traceability across the verification cycle
- ✓ Crunch simulation functional vectors with automated and optimized constraint and coverage generation
- ✓ Eliminate random stimulus debugging, enable functional stimulus grading and improve productivity
- ✓ Improve returns on your simulation investments – optimize simulation license and hardware requirements
- ✓ Formalize functional verification closure

WhizChip’s Verification Optimization Services -

- ✓ Is compatible with SystemVerilog, Vera, Verilog, VHDL, SystemC etc
 - Supports RVM, VMM, OVM ...
- ✓ Is completely non-invasive in nature
- ✓ Connects at any stage of your design verification activity
- ✓ Provides a seamless delivery model based on objective goals, with least involvement from your team



To reap the delivered benefits of WhizChip’s Verification Optimization Services and enjoy a predictable & early verification closure of your designs, please write to sales@whizchip.com

(C) Copyrighted information of WhizChip Design Technologies

WhizChip is a Semiconductor and System Design Services Company offering a broad spectrum of ASIC / SoC and related system design services & solutions to leading semiconductor and system design companies from around the world. Our unique expertise and customised / milestone based service engagement model makes us the most preferred vendor in semiconductor service industry. We bring benefits to our clients by working under a fixed cost model. It provides our clients a predictable environment in terms of both pricing and timelines. Read more about WhizChip at www.whizchip.com